While claims 1-26 were rejected under 35 U.S.C. § 102(b), Applicants respectfully submit that Sakaedani et al. has an effective reference date (i.e., a publication date) of December 2, 1998. Thus, Applicants respectfully submit Sakaedani et al. was not described in a printed publication (i.e., published) more than one year prior to the filing date of the present application (July 15, 1999). Accordingly, Applicants respectfully submit that Sakaedani et al. is not available as prior art under 35 U.S.C. § 102(b).

Assuming, arguendo, that Sakaedani et al. was available as prior art under 35 U.S.C. § 102(b), claim 1 is allowable over the cited references in that claim 1 recites a combination of elements including, for example, "level shifting means... to apply a first voltage level for turning off the thin film transistors to the gate lines upon power-on and to apply a higher voltage level than the ground voltage to the gate lines upon power-off." The cited references including Sakaedani et al., do not teach or suggest each and every element of the claimed invention. Accordingly, Applicants respectfully submit that claim 1 and claims 2-8, which depend from claim 1, are allowable over the cited references.

The Examiner cites Sakaedani et al. as teaching "a level shifting means by teaching an afterimage circuit 35 for receiving a power supply voltage and a ground voltage (see column 6, lines 21-26; column 4, lines 18-22, 53-58 through column 5, lines 1-10; column 5, lines 52-58 through column 6, lines 1-9)." (Office Action at 3) Applicants respectfully submit, however, Sakaedani et al. does not teach at least the aforementioned claimed elements, for example, "level shifting means... to apply a first voltage level for turning off the thin film transistors to the gate lines upon power-on and to apply a higher voltage level than the ground voltage to the gate lines upon power-off."

Claim 9 is allowable over the cited references in that claim 9 recites a combination of elements including, for example, "receiving a power supply voltage and a ground voltage to

apply a first voltage level for turning off the thin film transistors to the gate lines upon power-on." The cited references including Sakaedani et al., do not teach or suggest each and every element of the claimed invention. Accordingly, Applicants respectfully submit that claim 9 and claim 10, which depends from claim 9, are allowable over the cited references.

Claim 11 is allowable over the cited references in that claim 11 recites a combination of elements including, for example, "a gate voltage generator having a transistor connected between a first voltage source and a second voltage source to generate a gate-off voltage at an output." The cited references including Sakaedani et al., do not teach or suggest each and every element of the claimed invention. Accordingly, Applicants respectfully submit that claim 11 and claims 12-18, which depend from claim 11, are allowable over the cited references.

Claim 19 is allowable over the cited references in that claim 19 recites a combination of elements including, for example, "a gate-off voltage generator having a transistor connected between a first voltage source and a second voltage source to generate a gate-off voltage at an output." The cited references including Sakaedani et al., do not teach or suggest each and every element of the claimed invention. Accordingly, Applicants respectfully submit that claim 19 and claims 20-26, which depend from claim 19, are allowable over the cited references.

The Examiner cites Sakaedani et al. as teaching "a voltage generator circuit (34) that generates output voltages for the gate line driver circuit (33) (figure 3 at 33, 34)." (Office Action at 3) Applicants respectfully submit, however, Sakaedani et al. does not teach at least the aforementioned claimed elements with respect to claims 11 and 19.

Applicant believes the application is in condition for allowance and early, favorable action is respectfully solicited. Should the Examiner deem that a telephone conference would

further the prosecution of this application, the Examiner is invited to call the undersigned attorney at (202) 496-7500.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. § 1.136. Please credit any overpayment to deposit Account No. 50-0911.

Respectfully submitted,

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Date: November 22, 2002

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